Tracking Accelerating Spacecraft Signals with the Wide Dynamic Demodulator.

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ABSTRACT

The Wide Dynamics Demodulator (WDD) provides the capability to demodulate digital data received from an accelerating spacecraft, even during the high Doppler rates caused by booster engine firing.

The WDD is constructed around an internal microprocessor that receives high-level commands from the external system computer, interprets them to select the optimum tuning, filtering, and operating modes, and reports status back to the external computer. The WDD will acquire a 35 MHz input signal with up to ±4200 Hz offset from the estimated frequency, and the frequency may be changing by as much as ±8.2 Hz per second and at a rate of up to 30.6 Hz/second^2. The PN code is searched first, followed by Costas-loop carrier search. After carrier lock, the loop changes from first-order to third-order, allowing frequency changes of up to ±10,300 Hz from nominal at a rate of ±765 Hz per second. Data rates from 100 b/s to 300,000 b/s may be processed.

INTRODUCTION

The Wide Dynamics Demodulator evolved in response to the requirements of NASA's Tracking and Data Relay Satellite System (TDRSS) (see Ref. 1 and 2). During the orbital manuevers of TDRSS user satellites, the received Doppler frequency rate will rapidly shift when engine firing occurs. NASA studies predicted the motions of a large satellite-booster combination, thus also setting the equivalent Doppler frequency dynamics. A WDD feasibility study was chartered by Spacecom (the Space Communications Company), which developed the TDRSS System for NASA. This analytical study phase resulted in a follow-on study to create "breadboard" table-top circuitry for proof-of-performance evaluation. The final implementation phase created a prototype and six deliverable units.

This paper discusses the demodulator requirements, implementation, and performance, provides acquisition statistical analyses, and relates them to the communications requirements of powered spacecraft.

OVERVIEW

The Wide Dynamics Demodulator (WDD) is a digital data demodulator that was designed to support digital data transmissions of TDRSS user spacecraft, even though they may be under powered flight (see Ref. 3). This demodulator provides the capability to track rapid shifts in received carrier frequency and PN chip rate. The WDD will be used within the S-band Single Access Receive Equipment (SSARE) of the TDRSS White Sands Ground Terminal. The design is implemented in a chassis that will replace the existing Low Rate Demodulator (LRD). The WDD will fit within the same physical space and have the same basic electrical interfaces to the Automatic Data Processing Equipment (ADPE) computer system.

In order to enhance the concept of where the equipment fits into the system, refer to Figure 1. The Tracking and Data Relay Satellite System (TDRSS) consists of user spacecraft (such as the Shuttle), the supporting TDRS satellites, and the White Sands Ground Terminal (WSGT). The S-band signals from the user spacecraft are received by the TDRS satellite, where they are transponded to K-band for retransmission to the Ground Terminal in New Mexico.

As shown in Figure 2, the mesh single-access antenna of the TDRSS satellite receives the S-band incoming signals from the user spacecraft. After conversion to K-band, the space-to-ground-link antenna emits a K-band signal aimed at WSGT. This downlink signal is received by one of the 18 meter K-band antennas shown in Figure 3. After receipt at the White Sands Ground Terminal, the signals are downconverted to reduce the frequency to the 35 MHz IF frequency used by the demodulator.

A more detailed look at the signal flow is shown in Figure 4. The 18-meter-antenna signal is amplified by the low noise amplifier and downconverted to an S-band intermediate frequency. The signal is processed further to remove estimated Doppler and to develop the 35 MHz signal from the SSA converter/corrector to the Low Rate Demodulator (LRD). The WDD will replace the LRD in each of three identical equipment groups that support the North, Central, and South antennas. Two WDD's are used per group, one group for each antenna service.

BACKGROUND

User Spacecraft Dynamics

The orbit dynamics of a user spacecraft are relatively stable when there is no further rocket engine firing. The principal spacecraft velocity is that due to its nominal Keplerian orbit, although minor perturbations occur due to the ellipticity of the earth, planetary and lunar gravitational attraction, and the force of solar radiation. When a spacecraft is in this nominal stable orbit, the estimated spacecraft position and velocity are well known as a function of time, and accurate estimates of received Doppler frequencies and PN chip offset may be computed. These estimates are used in compensating the received signal, but residual dynamics exist that must be tracked by the demodulator. Occasionally, spacecraft maneuvers may be required, and the instant of firing may have as much as 9 seconds of time uncertainty as well as additional magnitude uncertainties. During the period that powered flight occurs, these signal uncertainties cause difficulties in effectively tracking the PN chip rate and carrier frequency.

There are five phases to a powered flight maneuver:

1. Essentially stable orbit dynamics prior to the beginning of powered flight.

2. Initiation of powered flight with major uncompensated acceleration uncertainties due to the uncertainties of engine thruster firing times and the realized magnitude of acceleration.

3. Nominal powered flight with minor acceleration uncertainies.

4. End of powered flight with major uncompensated acceleration uncertainties, as occurred in Phase 2.

5. Minor acceleration uncertainties after the powered flight is complete, as in Phase 1.

For example, a spacecraft/Inertial Upper Stage (IUS) combination ejected from the space shuttle orbiter will have orbital velocities only slightly different than that of the space shuttle. Booster firing will accelerate the combination with increasing velocity throughout the time of firing. When engine shut-down occurs, the acceleration will rapidly die out, perhaps in less than 1/2 second. The combination continues to coast in a new stable orbit that will be different from that at ejection from the space shuttle. At some later time, the explosive connector bolts will be fired, causing separation of the IUS from the spacecraft and possibly causing some slight acceleration due to the separation. Following separation, the spacecraft will assume a more predictable orbit.

The TDRSS software will make direct use of the NASA-supplied state vectors in commanding the communications equipment. These data permit nominal tuning and adjustment to minimize loss of data. For a user in an unstable orbit, NASA will provide a sequence of state vectors that represent user parameters at time intervals precisely 0.5 second apart. These data will provide a smooth sequence, such that the rates obtained from taking differences are consistent, contain no major irregularities, and do not induce an erratic behavior. While these state vectors are precise, the time at which each are applicable may be in error by as much as 9 seconds. During accelerations, the tracking receivers must maintain track in spite of the offsets in estimates that result from time uncertainty.

As shown in Figure 5, WDD Reacquisition Dynamics, the firing time uncertainty may cause as much as 9 seconds delay in the Doppler compensation. Most of the shift is corrected after compensation begins, but the residual acceleration effects appear in the demodulator input. These uncompensated dynamics then cause stresses on the demodulator tracking loops. While the WDD is designed to maintain track through these effects, loss-of-lock might occur. There are two points identified as "worst-case" locations: Case 1 during high acceleration, and Case 2 occurring immediately at the moment of engine firing. If signal tracking is lost, the WDD will independently start reacquisition procedures to attempt to regain lock on the spacecraft data. If lock of the PN and carrier tracking loops does not occur within 35 seconds, the loss-of-lock will be reported to the central computer equipment for further action.

The assessment of the maximum spacecraft dynamics was made by Mr. Les Riddle of NASA/WEC at Goddard Space Flight Center. The combination of the Galileo satellite under orbital injection by the 5000 pound thrust Inertial Upper Stage (IUS) was selected to bound the requirements. Figure 6 depicts the acceleration profile over the IUS firing. The initial jerk (acceleration rate) occurs at ignition, and full thrust then smoothly builds up in 75 seconds, followed by a rapid, smooth decrease. As the acceleration increases, the rate of change of Doppler also increases, thus stressing the third-order Costas tracking loop of the WDD. If the tracking phase error becomes excessive, the WDD will lose lock.

Because of the engine firing, flame attenuation of the signal may occur, possibly to less than required for acquisition. Since the WDD retains the PN offset and carrier offset values at loss-of-lock, reacquisition is possible where acquisition would not be.

From these acceleration dynamics, maximum frequency offset was estimated at $\pm$4.54 kHz while the maximum frequency rate was estimated at $\pm$68.9 Hz/second. The maximum PN code offset was estimated at 182 chips. The specifications were established somewhat higher, at $\pm$6 kHz offset, $\pm$70 Hz/second frequency rate, and $\pm$200 chip PN code offset.

System Aspects

The WDD design avoids the need for changes in the Automatic Data Processing Equipment (ADPE) software. Through the use of similar interfaces, the WDD may function while using what appear to be LRD commands. A minor computer interface requirement was that the Service Control Unit (SCU) required the addition of an extra connector to allow the WDD to recognize commands being sent to the Low/Medium Rate Bit Synchronizer, the Low Rate Bit Synchronizer, and the Combiner. With these extra command signals, the WDD can identify and interpret signals that are going to the other units just mentioned. This approach permits the correct setup of internal WDD circuitry to be inferred by the information in the setup data to the other bit syncs or combiner (the so-called "expert system" form of artificial intelligence).

Another design consideration was that the WDD and its power supply must fit within the available space when the LRD receiver is removed. Cooling and power requirements had to be less than for the LRD.

In a broader sense, the design was made adaptable for a conversion to a replacement of the Multiple Access Ground (MAG) Receiver and the K-Band Data Demodulator (KDD). Considerable saving in maintenance and logistics could be obtained if a similar variant of the WDD could be substituted for these other receivers. The modular design of the WDD would thus require replacement of only a few cards to provide adaptability to 26 other demodulator units, for a total of 32 similar receivers. This approach would also permit adaptation to non-TDRSS systems.

PROGRAM PHASES

A task of this magnitude should be divided into distinct phases to allow decision points for continuing the development. A three-phase procurement plan was developed during the first quarter of 1980. Phase I was to be a short 2-month feasibility study to determine if the specification could be met and to create a proposal for Phase II, a definition phase. During this phase, additional analysis would be performed and breadboard hardware would be built to prove out the design in those areas of high risk. This phase would also develop a specification, Statement of Work, and proposal for phase III.

Phase III was the hardware implementation phase, which would result in the design, construction, and testing of six WDD's.

Studies were performed by the Harris SATCOM Modem section and by Motorola. The hybrid design, using a digital third-order tracking loop, was chosen for further evaluation.

The breadboard definition phase evaluated flatplane circuitry to find the cycle slip rate of the carrier tracking loop in the presence of frequency dynamics, as well as bit error rate and acquisition times. This experiment required the development of a flexible dynamics generator to drive the demodulator with a strenuous test signal.

Carrier loop results showed the specifications for cycle slip and loss-of-lock could be achieved with some margin even in the presence of "uncompensated" dynamics. However, the tests proved that a second-order loop was not adequate.

PN code acquisition and tracking was also breadboarded. Code tracking performance was satisfactory, but acquisition results showed more extensive processing algorithms were needed to give protection against false locks at high SNR.

The implementation phase developed the concepts of the earlier studies into a usable, reproducible demodulator. A prototype of superficially identical appearance, construction, and performance was created to allow evaluation of the design. The course of development was monitored through technical reviews involving NASA, NASA/WEC, TRW, STI, Spacecom, and Harris. During this phase, the early dynamics generator was expanded into a three-chassis group of Special Test Equipment (STE) to provide a microprocessor-controlled signal source.

Physical and Electrical Interface Characteristics

The WDD had to fit within the space of the existing demodulator, and was to be compatible with existing electrical interfaces. The software interface also had to be satisfied.

The appearance of the WDD Receiver chassis is shown in Figure 7. The power supplies are contained in a smaller chassis, thus keeping line voltage and stray ac out of the receiver. The receiver is remotely-controlled by the TDRSS ADPE (Automatic Data Processing Equipment) computer; only a maintenance reset pushbutton is on the front panel. While the unit will operate in a closed cabinet where the Test Controller cannot see it, a profusion of indicator lamps were provided as a diagnostic aid for maintenance personnel.

The receiver contains two card files: PN tracking and microprocessor, and IF Carrier. Two fans provide air flow from back to front, cooling the cards adequately even when the covers are removed.

The electrical interfaces of the WDD receiver are shown in Figure 8. These electrical interfaces are as follows:

a. AC Power Input: (DC power is supplied from the WDD Power Supply into the receiver chassis.)
b. IF Input: The IF input will be a nominal 35 MHz carrier containing PN spread and clear phase modulated signals.
c. R&RR (Range & Range Rate) Interface: An epoch event signal and PN clock are made available to synchronize the R&RR logic (range extractor) with the despreader's PN code

sequence after the acquisition has been obtained.

d. Reference Interface: The CTFS timing subsystem will provide a 5 MHz station standard frequency reference and a 1 pps timing pulse for time reference.

e. Data Output Interface: The I and Q output consists of the demodulated baseband data signals to the bit synchronizers.

f. Service Control Interface: The WDD receives all setup and control data from the ADPE via the Service Control Unit (SCU) and returns status data to the ADPE via the SCU.

g. Recovered Carrier Interface: The recovered carrier reference is 35 MHz.

Electronic Implementation

The conceptual block diagram of Figure 9 shows the logical functions of the receiver.

The 35 MHz input signal enters the INPUT circuitry at the upper left. A synthesized reference of approximately 15 MHz is used to obtain a 20 MHz signal for the EARLY/LATE DESPREADER, while a filtered and amplified 35 MHz signal is applied to the ON-TIME DESPREADER. When the PN loop is tracking, the incoming signal is despread and passed to the FILTERS AND MIXER. If the PN loop were searching, the PN sequence would be stepped 1/2 chip at a time until a sufficient correlation occurred and the PN lock was declared. The derived PN epoch and clock are provided to the Range and Range Rate Equipment.

In the digital carrier loop, a numerically-controlled oscillator is used to generate approximate 5, 20, 30, and 35 MHz signals. The 35 MHz signal is the recovered carrier, a regenerated clean signal. The 20 MHz signal is used to derive four precise sampling points along the incoming 5 MHz signal. (This signal was hetrodyned from the 35 MHz despread signal and the synthesized 30 MHz.) These points sample (ideally) the positive and negative peaks and the zero-crossings of the carrier. If a phase error is present, the "zero" samples will be of different values, and their difference is representative of the sign and magnitude of the phase error. The loop is then driven to obtain an average difference of zero. When the loop is tracking, the peak sample points are properly aligned, and an AGC level can be coherently derived from the peak-to-peak measurement.

The 5 MHz signal is also split off to drive the DATA DETECTORS, where the actual demodulation occurs. The coherent 5 MHz recovered carrier is combined with the 5 MHz signal, resulting in baseband digital data that is output to the external bit synchronizers.

The operation of the WDD is directed by the microprocessor-based Controller, which receives instructions from the ADPE, and outputs status information to ADPE. The internal signals required by the WDD are synthesized from the 5 MHz input from the CTFS (Common Time and Frequency Standard).

To expand upon a few of these functions, all internal frequency sources are synthesized from the incoming 5 MHz, thus assuring accuracy of $\pm 7 \times 10^{-12}$. When a spacecraft transmitter is slaved to the Ground Terminal by a pilot tone, two-way Doppler

measurements are possible.

NASA Data Signals

The NASA standard data groups and modes provides a number of distinct operational set-up conditions (see Table 1). In Data Group 1, Mode 1, both the I and Q (quadraphase) channels are spread by a PN code of sequence length $(2^{10} - 1) \times 256$. The PN sequences are identical, but the Q code lags the I code by more than 20,000 chips (code elements) allowing ambiguity resolution. The chip timing is also staggered one-half chip (SQPN code). These codes are set by changing the register feedback taps in response to commands from the ADPE computer.

During acquisition, the PN code is searched in 1/2-chip increments in an optimal search algorithm.

In Data Group 1, Mode 2, the PN code is only 2047 chips along, and rapid acquisition is possible. These Gold codes differ for the I and Q channels, thus reversed channel lock cannot occur.

In Data Group 1, Mode 3, the I channel code is the same as in Mode 1, but the Q channel is not spread (called "clear" or uncoded).

A Data Group 2 function is available, providing a BPSK channel.

The search time is reduced by using a computer estimate of the delay in receipt of the PN code epoch, an all 1's condition. A maximum value of 16.77 seconds is possible. When the epoch delay time has passed, the PN generator begins counting, and the PN search process begins. When the detector senses code alignment, tracking begins, and the incoming signal can be "despread" of its PN sequence.

A digital carrier tracking loop samples the signal and steers a Numerically-Controlled Oscillator 'NCO) to obtain and maintain phase lock. A first-order bit-decision-aided, Costas phase lock loop is used for acquisition, but is then changed to a third-order loop to permit tracking during spacecraft accelerations. Since frequency uncertainties are present, the 73 Hz tracking bandwidth is necessarily wider than for a standard demodulator.

Table 1. WDD Data Characteristics

DATA GROUP 1	
Spread Spectrum PN QPSK	
Mode 1:	Supports two-way Doppler ranging
Mode 2:	Supports one-way Doppler ranging Q code differs from I code
Mode 3:	I is PN coded BPSK Q is clear BPSK I/Q power ratio may range from 1:1 to 1:4
PN Code Family:	STDN 108 18-stage shift register sequence for Modes 1 and 3; STDN 108 Gold codes for Mode 2
PN Code Offset:	Q code delayed X +1/2 PN chips, where X $\geq$20,000 chips
DATA GROUP 2	
Unspread	

NOTES

1. Any signal may be coded or uncoded, as well as NRZ or Biphase.
2. Data formats may be Level, Mark, or Space

When the carrier loop is locked, a 5 MHz carrier is recovered for synchronous

demodulation of the I and Q signals. If carrier lock is lost, reacquisition search begins using the last values for PN and carrier NCO control to speed the search process.

Special Test Equipment (STE)

There are three STE chassis that perform the dynamic signal generation required by the WDD. These chassis also provide the command functions required for the WDD and the Low/Medium Rate Bit Synchronizer. These three units consist of the Controller Chassis, the Dynamics Chassis, and the C/N_0 Test Set. The Controller provides the point to enter data into the STE microprocessor and to receive an indication of signal strength and status from the WDD. The dynamics chassis generates the PN signals and provides the proper rates of change of slewing. The C/N_0 Test Set provides the carrier frequency at 35 MHz that is also subject to frequency offset in simulating the variability of received Doppler from a spacecraft that is in powered flight. Since the carrier and PN effects must be varied simultaneously, the Controller commands both units in synchronism. Other auxiliary commercial test equipment is used to complete the STE setup, as shown in Figure 10.

Operation of the STE is facilitated by a computer program written for an HP desk top computer. The specification requirements are built into the program, and the output provides switch and dial setting recommendations for STE set-up. When acquisition is complete, the operator enters the observed times into the computer for logging and data reduction.

PERFORMANCE CHARACTERISTICS

When the WDD is installed, normal spacecraft data and tracking services will be provided in approximately the 100 to 300,000 symbols/second range. The WDD can provide demodulation of both Viterbi-coded and uncoded signals, in either the Non-Return-to-Zero (NRZ) or biphase format. When 1/2-rate Viterbi-coded signals are processed, two adjacent symbols are required to define one data bit. The WDD processes these symbols the same as uncoded bits, but the maximum data rate is halved.

Performance characteristics have been measured with the prototype and with the first deliverable WDD. Table 2 shows a synopsis of performance. Testing concentrated on the most stressing modes of operation in order to limit the number of tests required. Peculiar values of symbol rates were often used to test at a point where passband filtering is close to filter point, thus obtaining a conservative performance estimate.

Many of the parameters are probabilistic in nature, and test results are not likely to be repeatable. Some of these parameters are loss-of-lock rate, cycle slip rate, and the acquisition and reacquisition times. Numerous repetitions were required in order to gather a statistically adequate sample. This paper demonstrates the use of Weibull graphic analysis of the cumulative distribution function of some of these parameters.

Table 2. Performance Characteristics

Inputs

Minimum C/N_0 Levels (dB-Hz):				
Mode	Coded		Uncoded	
	NRZ	Biphase	NRZ	Biphase
DG1-1	39.5	40.6	42.8	42.8
DG1-2	39.1	39.5	44.3	44.3
DG1-3; 1:1	39.5	40.6	43.3	43.3
DG2	38.5	39.6	43.3	43.3

Input Frequency
35 MHz (standard)

Input Total Power
-37 dBm to -10 dBm

Data Rates
100 S/s to 300 kS/s (NASA DG1-1,3)
1 kS/s to 300 kS/s (NASA DG1-2)
1 kS/s to 100 kS/s (NASA DG2)

Performance
Acquisition probability: >90%
Acquisition time: median <5, 15, 45 s (mode dependent)
Reacquisition time: median <20 s
Cycle slip time: mean time >90 minutes
Loss-of-lock: <1 per 100 acceleration events at minimum C/N_0 levels
Recovered carrier phase noise: <1° over 10 Hz to 200 kHz for C/N_0 >70 dB-Hz
Error rates (with LMRBS)
Bit: 5×10^{-6} at E_s/N_0 = 14.3 dB
Symbol: 0.036 at E_s/N_0 = 6.1 dB
PN clock jitter: <14 ns
PN epoch delay variation: <±13 ns

Worst-case performance normally occurred when processing NASA Data Group 1, Mode 1 signals (spread long-code PN); most testing used this signal to obtain conservative performance estimates. All testing was done with Manchester II coded signals since uncoded signals would be processed with equal facility. This coded approach cut the potential test case universe in half.

Acquisition Time

The acquisition time is strongly dependent upon the signal group and mode, and upon the symbol rate. The specified value is also a function of C/N_0. A complicating factor is that the time is also probabilistic, thus each test must be run many times to obtain a realistic performance estimate. The specification required that, of the test trials attempted, 90 percent or more must acquire, and 50 percent or more of successful acquisitions must occur in less than the specified time. While the specification uses 50 percent of successful acquisitions, the test used 50 percent of all attempts, and thus yields a more conservative estimate.

The carrier frequency offset and the PN code offset were selected from a range and appropriate distribution of values, and the acquisition times were collected using this random process. All modes, rates, and C/N_0 values tested were compliant with the specification. These tests represent the modes that are most stressing to the WDD. The worst-case test result occurred with Data Group 1, Mode 1 using a minimum C/N_0 signal of 39.5 dB/Hz. In this case, 57 percent of the acquisition times were less than the specified time. All tests met the 90 percent acquisition requirement. The test of predetection combining of I and Q channel power with 3 dB less power per channel still yielded performance comparable to that at the 3 dB higher "minimum" C/N_0 level. The theoretical 3 dB combining gain thus had been realized.

Table 3 shows a set of 36 acquisition trials results arranged in descending rank order. From this list, the cumulative distribution function has been derived and plotted in Figure 11. The distribution is clearly bimodal, showing a segment up to 15 seconds, followed by a separate sloping segment above 15 seconds. The higher value segment is fitted with a straight line representing an exponential distribution, and represents a more dispersed random mechanism. The lower segment represents the normal performance of acquisition, which has a limited dispersion.

While the mean time is 14.76 seconds, the median time is only 10.9 seconds. The median is a more robust measure of performance, as 72.2% of the times are less than the 15 second specification.

A second data set is plotted in Figure 12, where an intermediate distribution is seen around 50 to 80%. The mechanism of this segment is probably the same as in the lower segment, but a delay of approximately 7 seconds has shifted the data distribution.

Table 3. Acquisition Times
WDD No. 2; Ranked Results; N = 36
DG1-1; Spec: 50% ≤ 15 seconds

n	Time	Percentile
36	45.4s	100
35	36.1	97.2
34	33.9	94.4
33	27.9	91.7
32	25.2	88.9
31	21.8	86.1
30	19.7	83.3
29	18.5	80.6
28	18.3	77.8
27	16.7	75.0
26	14.7	72.2
25	12.0	69.4
24	11.9	66.7
23	11.9	63.9
22	11.8	61.1
21	11.7	58.3
20	11.6	55.6
19	11.0	52.8
18	10.9	50.0
17	10.8	47.2
16	10.8	44.4
15	10.7	41.6
14	10.3	38.9
13	10.2	36.1
12	10.1	33.3
11	10.0	30.6
10	9.9	27.8
9	9.5	25.0
8	9.5	22.2
7	8.9	19.4
6	8.7	16.7
5	8.6	13.9
4	8.5	11.1
3	8.1	8.3
2	8.1	5.6
1	7.7	2.8

Mean = 14.76s; 72.2% ≤ 15s
Std. Dev. = 8.8s; Median = 10.9s

Cycle Slip/Loss-of-Lock

The cycle slip (see Ref. 4) and loss-of-lock tests were run using minimum C/N_0 input signals with a dynamically varying frequency as shown in Figure 13. Normally, one trapezoidal profile would take 30 seconds for a cycle simulating spacecraft booster engine firing. Special tests demonstrated that the profiles stressed the carrier tracking loops at the trapezoid corners. This indicated that the profile could be shortened to a 4-second cycle, allowing the test to be run more quickly. Actual test times could then be multiplied by 30/4, or 7.5, to estimate the mean-times for the specified long-period profile. The profile is also more stressing than will actually occur, as the corners are exact without rounding, thus simulating an infinite jerk rather than the ± 30.6 Hz/s^2 of the specification. The cycle slip and loss-of-lock tests were consolidated by using peak frequency accelerations of ± 750 Hz/s rather than the ± 330 Hz/s specified for the cycle slip time.

At minimum C/N_0, no cycle slips or loss-of-lock occurred in a 36-minute period. Earlier prototype experiments were run with C/N_0 values of 3 dB and 3.5 dB below the "minimum" value. There is no precise noise threshold, but loss-of-lock is probabilistic; see Ref. 6. Loss-of-lock times are shown in the cumulative distribution of Figure 14. The exponential mean is equal to the standard deviation, and for these C/N_0 values, are equal to 5.6 minutes at -3.5 dB and 12.5 minutes at -3 dB relative to the specified minimum. A line plot of the 90 minute mean distribution is also shown. (Cycle-slipping is exponentially distributed; see Ref. 7, Holmes, page 95, equation 4.4-6.)

Bit Error Rate/Symbol Error Rate

The WDD Symbol Error Rate (SER) performance is specified in conjunction with the Low/Medium Rate Bit Synchronizer with which the WDD is used. The results are then compared to the theoretical error curve shown in Figure 15 (see Ref. 5). Without signal dynamics, performance tends to be approximately 1 dB worse than theory (a 1 dB higher than theoretical C/N_0 is required for a given error rate).

When both data jitter and dynamics are present, the SER varies with symbol rate as shown in Figure 16. The data samples show that the worst SER is about one-half the design goal of 0.029 and about one-third of the specified 0.036.

Symbol Error Distribution

A special test was performed to evaluate the time distribution of the symbol errors. The time of each error occurrence was marked by a strip chart recorder. The time intervals between errors were then ranked and a Weibull plot generated (see Figure 17).

Theoretically, the error occurrences are random and independent (a Poisson process), thus the time between consecutive errors should have an exponential distribution. In a Weibull distribution, the slope coefficient is used to infer the likely distribution of the data. A slope of 1.0 will provide a good fit to exponentially-distributed data, and indeed it does for the test data. About 2% of the data had a time interval shorter than the exponential fit would suggest, but the resolution of the recorder limited the visible difference to 38 ms.

A plot of the data of Figure 17 may also be constructed on the more common semi-logarithmic graph paper of Figure 18. The left scale is the probability that the time difference will be more than the indicated time difference (Δt). The right scale is the probability that the time difference will be less than or equal to the Δt. The exponential line fit must pass through the 100% > 0 seconds corner of the graph, and the determining constant, ΔT, is found where the line crosses the 1/e% point, 36.79%. This value is approximately 1.3 seconds.

The precise value is found from the line equation:

$$Pr\ (T > \Delta t) = 100e^{-(\Delta t/\Delta T)}$$

where $Pr\ (T > \Delta t)$ is the probability of a value T exceeding the Δt level. From the lower right line intercept (5.96 seconds, 1%),

$$1\% = 100e^{-(5.96/\Delta T)}$$
$$0.01 = e^{-(5.96/\Delta T)}$$
$$\ln 0.01 = \ln e^{-(5.96/\Delta T)}$$
$$-4.60517 = -5.96/\Delta T$$
$$\Delta T = 5.96/4.60517$$
$$\Delta T = 1.292 \text{ seconds}$$

Therefore, other levels may be estimated from:

$$Pr\ (T > \Delta t) = 100e^{-(\Delta t/1.292)}$$

Reacquisition Time

Reacquisition time was measured at a C/N_0 of 43.7 dB-Hz and a symbol rate of 5800 S/s. Both biphase and NRZ data formats were used in testing. Reacquisition searches are based upon the last measured values of carrier offset and PN code offset, thus the search range can be reduced, speeding reacquisition time. The design goal (not specification) was 20 seconds or less, median, while

the maximum observed time was 14 seconds. These tests were run using the dynamics profiles shown in Figures 19 and 20. The STE synchronously varies the carrier frequency and the PN code chip rate to simulate the spacecraft signal that is received.

The reacquisition times for the deliverable WDD are shown in Table 4. These times were ranked in descending order to estimate the probability percentiles shown. The percentiles are estimates of the reacquisitions where the time is equal to or less than the indicated percentile. The distribution is plotted in Figure 21, and is not exponential in nature. (The Weibull graph paper allows estimation of the nature of the distribution.) Many more trials would be required to estimate the distribution with confidence, but there appear to be multiple Gaussian processes present.

Table 4. Unit 1 Reacquisition Times

Trial	Time	Ranked Times	Pr (T > Value) Percentile
1	9s	14s	100%
2	11	14	91.7
3	9	12	83.3
4	14	11	75.0
5	9	11	66.7
6	11	11	58.3
7	9	9	50.0
8	11	9	41.7
9	9	9	33.3
10	12	9	25.0
11	9	9	16.7
12	14	9	8.3

Median Time = $\frac{9 + 11}{2}$ = 10 seconds

NOTE: Odd trials take 3 seconds less time than even trials due to the direction of search.

PRESENT STATUS

The WDD prototype has now passed through extensive testing and evaluation, and the design team is confident that the design can be successfully implemented in the production of the deliverable units. Several demodulators have now passed acceptance testing and have been shipped to WSGT. The WDD installation at the White Sands Ground Terminal will be completed in mid-1984. Following the completion of the assembly and test of all units at the Harris plant, the Special Test Equipment (STE) will also be delivered to WSGT for use in the new Maintenance Depot.

CONCLUSION

The Wide Dynamics Demodulator brings a new level of advanced tracking performance to the NASA TDRSS program. The design has now been implemented and tested in the laboratory, thus bringing to satellite communications a capability to maintain signal tracking and demodulation through the orbital injection phase without loss-of-lock. With the WDD, data collection and communication can be maintained through the swift acceleration of powerful spacecraft boosters, such as the Inertial Upper Stage (IUS). This ability to maintain spacecraft contact during pronounced vehicle motions will ensure enhanced control of vehicle motions. This capability will be of great significance when a ground-based pilot is controlling the Orbiting Manuevering Vehicle (OMV, the "Space Tug"), when continuous data coverage is required to assure safety when docking the OMV to the Space Station.

As the Nation's space program expands into the coming century, the greater communications availability of the WDD will ensure satisfaction of the user community's needs.

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(1) Anon., "Performance Specification for Telecommunications Services (NASA S-805-1 MOD)", Western Union, 1976.

(2) Anon., "Tracking and Data Relay Satellite System (TDRSS) Users' Guide", NASA Goddard Space Flight Center, Greenbelt, Maryland, January, 1980.

(3) Anon., "Wide Dynamics Demodulator Familiarization Guide", Harris Corporation, Melbourne, FL, August 1983.

(4) Spilker, J.J., Digital Communications by Satellite, Prentice-Hall, Inc., 1977, p. 380.

(5) Roden, M.S., Digital and Data Communications Systems, Prentice-Hall, Inc., 1982, p. 305.

(6) Gardner, F.M., Phaselock Techniques, Second Edition, John Wiley & Sons, New York, 1979, p. 36.

(7) Holmes, J.K., Coherent Spread Spectrum Systems, John Wiley & Sons, New York, 1982, p. 95, 130, 150.

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The careful text preparation by Ms. Willean Bell is greatly appreciated.

APPENDIX

SIGNAL DYNAMICS

The following Tables A-1 through A-3 show the specification dynamics requirements for the WDD. In a stable orbit, the Doppler shift is predictable, and a convertor/corrector restores the IF to a nominal 35 MHz. The uncertainty remaining results in the residual dynamics shown in the upper three rows.

In Powered Compensated orbits, a greater uncertainty exists due to the variation in booster engine thrust and the time of occurrence.

In Powered Uncompensated orbits, the dynamics are the most severe, and result principally from the compensation being delayed in starting due to the uncertainty of exact firing time. The STE is capable of generating each of the dynamics profiles required to validate the specified performance.

Table A-1. Maximum ¯F Frequency Dynamics

MODES	ORBIT DYNAMICS TYPE	MAXIMUM FREQUENCY UNCERTAINTY f (kHz)	MAXIMUM FREQUENCY RATE $\dot{\Delta f}$ (Hz/s)	MAXIMUM FREQUENCY ACCEL $\ddot{\Delta f}$ (Hz/s^2)
DG-2 Mode 3 DG-1 Mode 1 and 3	Stable	±2.2	±2.5	±0.002
DG-1 and DG-2 Mode 2A	Stable	±1.9	±8.2	±0.001
DG-1 and DG-2 Mode 2B	Stable	±4.2	±8.2	±0.001
DG-2 Mode 3 DG-1 Mode 1 and 3	Powered Compensated	±10.3	±330	±3.1
DG-1 and DG-2 Mode 2A	Powered Compensated	±6.5	±165	±1.5
DG-1 and DG-2 Mode 2B	Powered Compensated	±8.8	±165	±1.5
DG-2 Mode 3 DG-1 Mode 1 and 3	Powered Uncompensated	±10.3	±765	±30.6
DG-1 and DG-2 Mode 2A	Powered Uncompensated	±6.5	±383	±16.6
DG-1 and DG-2 Mode 2B	Powered Uncompensated	±8.8	±383	±16.6

Table A-2. Frequency Dynamics for Acquisition and Reacquisition

MODES	ORBIT DYNAMICS TYPE	MAXIMUM FREQUENCY UNCERTAINTY f (kHz)	MAXIMUM FREQUENCY RATE $\dot{f}$ (Hz/s)	MAXIMUM FREQUENCY ACCEL $\ddot{f}$ (Hz/s^2)
DG-2 Mode 3 DG-1 Mode 1 and 3	Stable (Acquisition)	±2.2	±2.5	±0.002
DG-1 and DG-2 Mode 2A	Stable (Acquisition)	±1.9	±8.2	±0.001
DG-1 and DG-2 Mode 2B	Stable (Acquisition)	±4.2	±8.2	±0.001
DG-2 Mode 3 DG-1 Mode 1 and 3	Powered Compensated (Reacquisition)	±6.0	±70	±3.1
DG-1 and DG-2 Mode 2A	Powered Compensated (Reacquisition)	±3.7	±42	±1.5
DG-1 and DG-2 Mode 2B	Powered Compensated (Reacquisition)	±6.0	±42	±1.5

Table A-3. Maximum PN Code Dynamics for Reacquisition*

MODES	ORBIT DYNAMICS TYPE	MAXIMUM** INITIAL CODE OFFSET (CHIPS)	MAXIMUM FREQUENCY UNCERTAINTY (CHIPS/SEC)	MAXIMUM FREQUENCY RATE (CHIPS/SEC^2)	MAXIMUM FREQUENCY ACCELERATION (CHIPS/SEC^3)
DG-2 Mode 3 DG-1 Mode 1, 3	Stable	$\pm$100	$\pm$3.0	$\pm$0.0033	$\pm 0.26 \times 10^{-5}$
DG-1 and DG-2 Mode 2A	Stable	$\pm$60	$\pm$2.5	$\pm$0.011	$\pm 0.13 \times 10^{-5}$
DG-1 and DG-2 Mode 2B	Stable	$\pm$90	$\pm$5.7	$\pm$0.011	$\pm 0.13 \times 10^{-5}$
DG-2 Mode 3 DG-1 Mode 1, 3	Powered Compensated	$\pm$200	$\pm$8.2	$\pm$0.095	$\pm$0.0042
DG-1 and DG-2 Mode 2A	Powered Compensated	$\pm$110	$\pm$5.0	$\pm$0.048	$\pm$0.0021
DG-1 and DG-2 Mode 2B	Powered Compensated	$\pm$140	$\pm$8.2	$\pm$0.048	$\pm$0.0021

*Acquisition not required during uncompensated dynamics.

**Initial code offset for stable orbit acquisition after loss-of-lock is based on a maximum user acceleration of 14.8 m/sec^2. Therefore, the actual maximum offset is 82 chips for Modes 1 and 3.

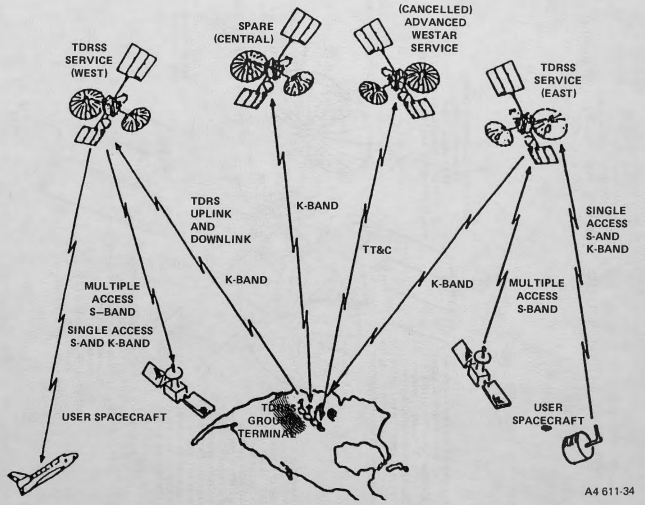

Figure 1. Tracking and Data Relay Satellite (TDRS) System. User spacecraft data are relayed through TDRS to and from the New Mexico Ground Terminal.

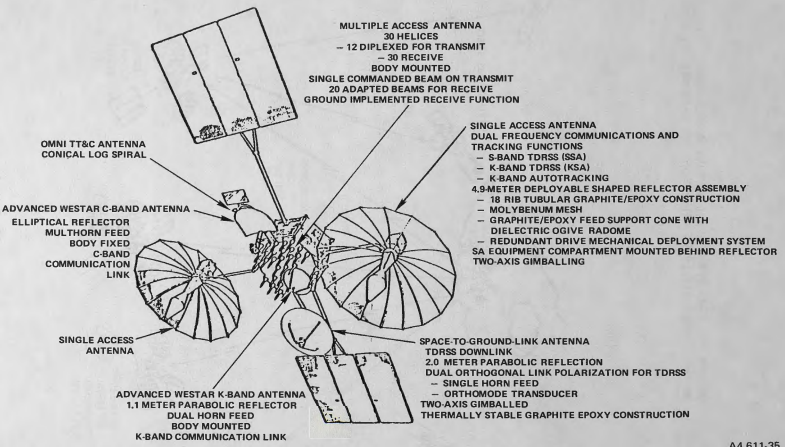

Figure 2. Tracking and Data Relay Satellite (TDRS). Single access antennas point to one spacecraft each; the multiple access array can service 20 users.

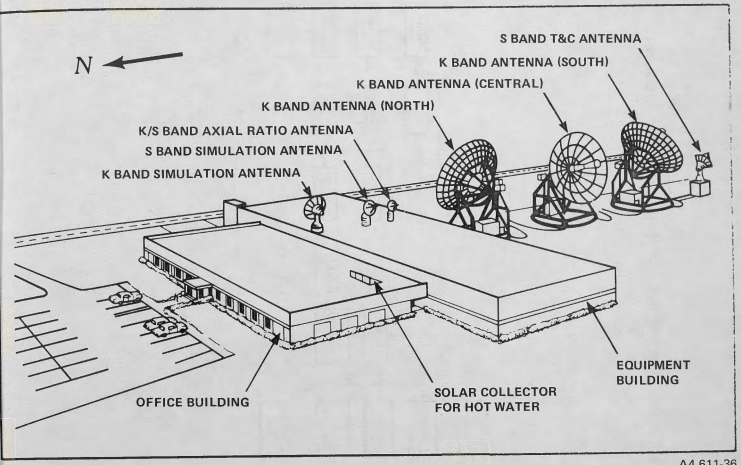

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Figure 3. White Sands Ground Terminal (WSGT). Each of the K-Band antennas will point to a TDRS spacecraft.

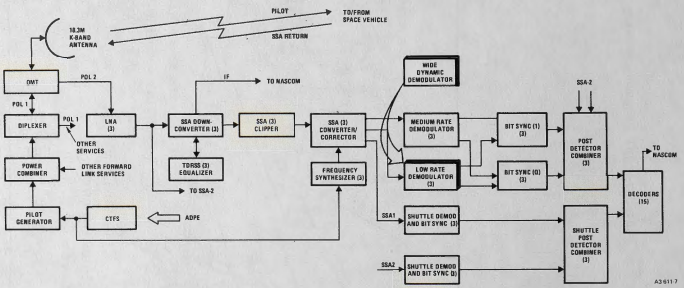

Figure 4. SSAR Block Diagram. The WDD will replace the existing Low Rate Demodulator.

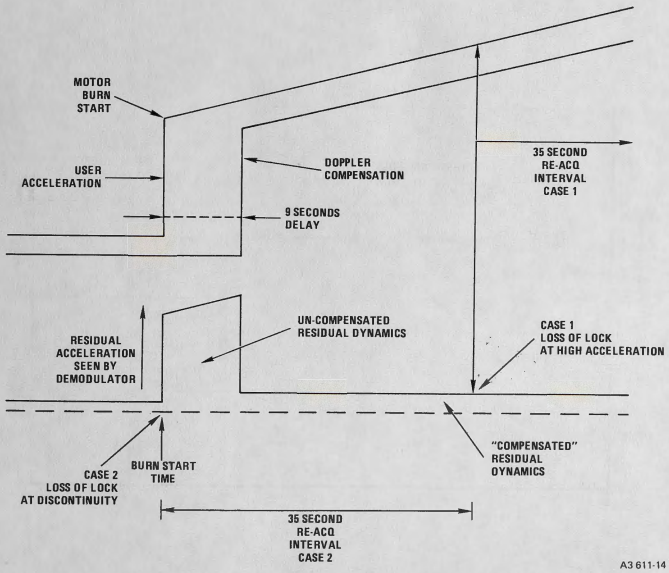

Figure 5. WDD Reacquisition Dynamics. Firing uncertainties may cause imperfect doppler compensation. The residual dynamics may stress a phase-lock-loop to lose lock.

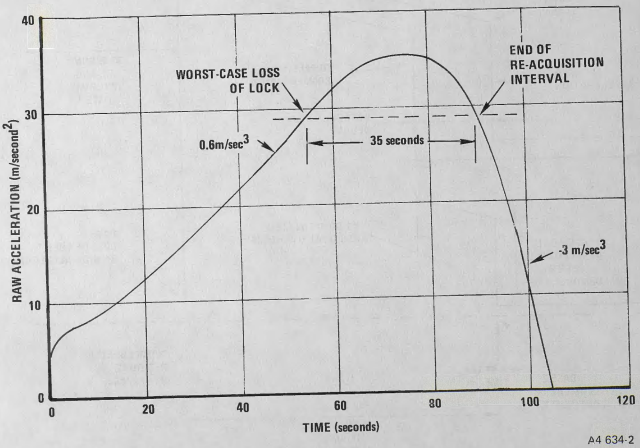

Figure 6. Galileo/IUS Acceleration Profile. This profile was used to determine the WDD tracking requirements.

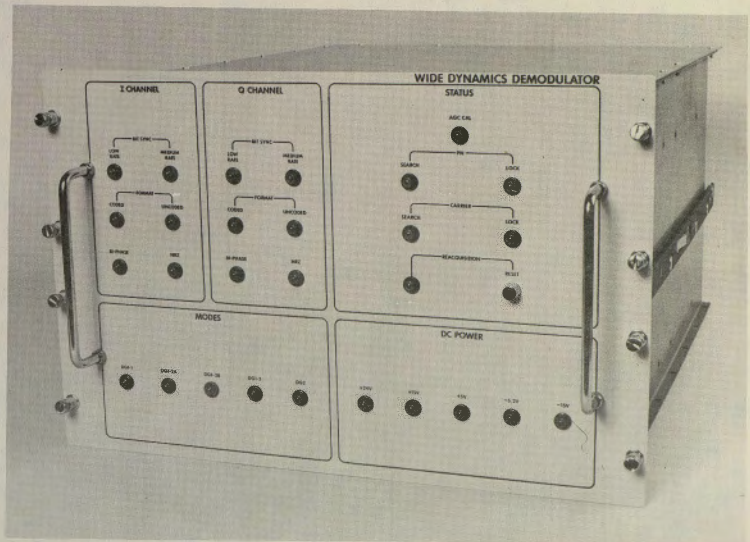

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Figure 7. The WDD Receiver Chassis. The panel indicates status for ease of checkout.

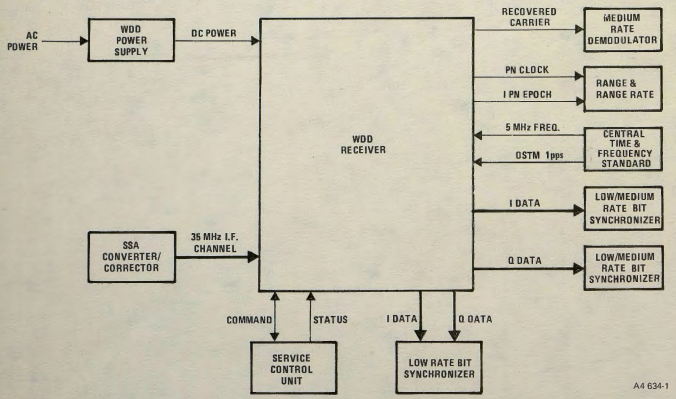

Figure 8. Electrical Interfaces. The WDD provides data to two types of bit synchronizers.

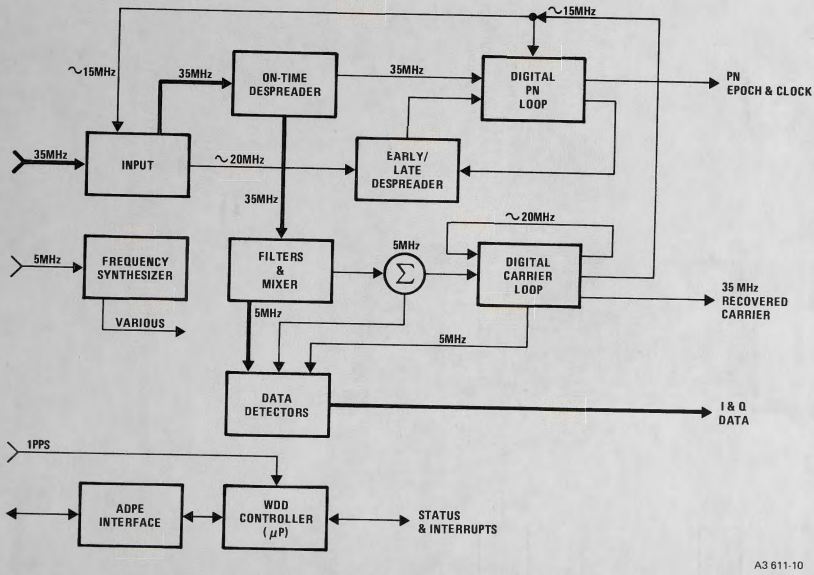

Figure 9. WDD Conceptual Block Diagram. The signal is despread by the PN loop, and tracked and demodulted by the carrier loop circuits.

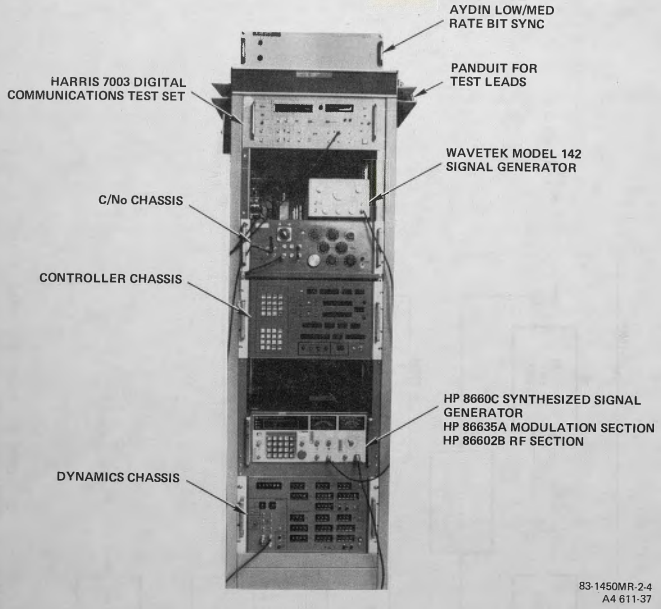

Figure 10. STE Rack Equipment. The deliverable STE and nondeliverable recommended test equipment were consolidated in one rack to facilitate testing.

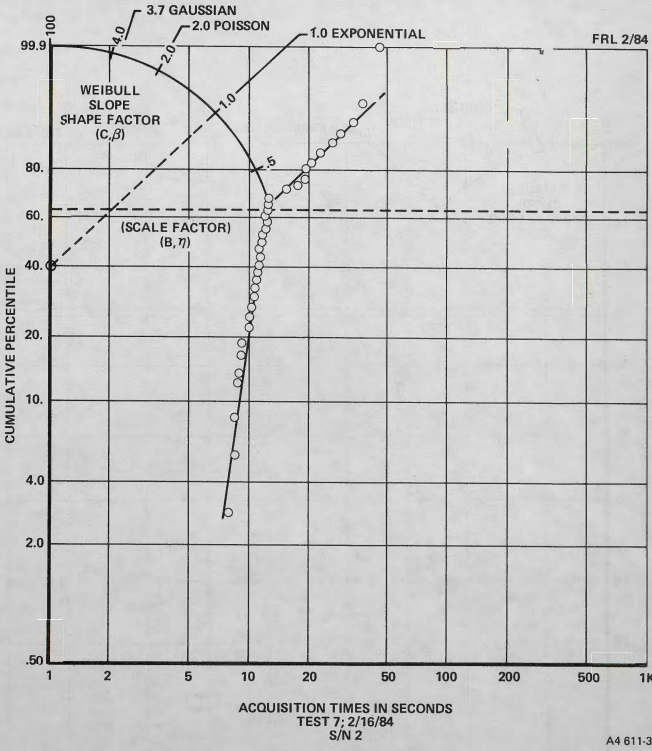

Figure 11. CDF of Acquisition Times; Test 7; 2/16/84; S/N 002. The two line segments indicate a random distribution is combined with a narrower-than-Gaussian distribution.

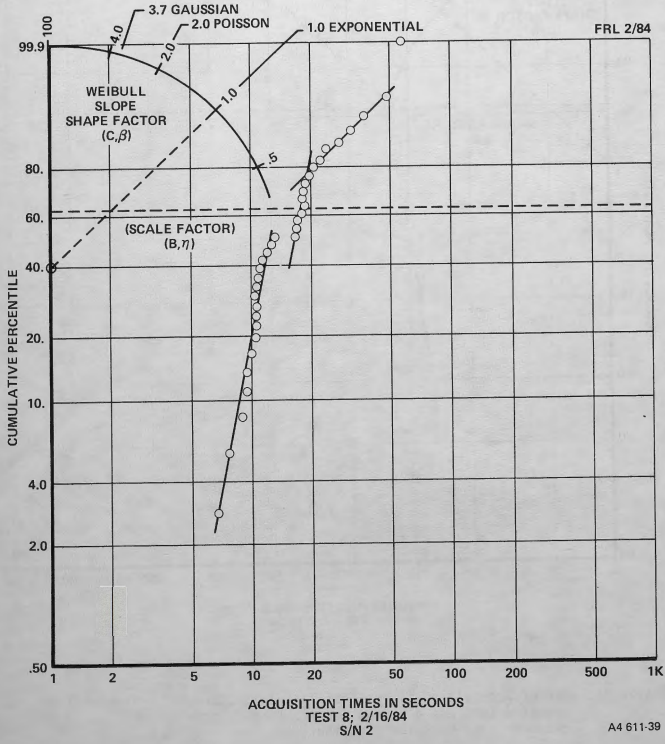

Figure 12. CDF of Acquisition Times; Test 8; 2/16/84; S/N 002. A parallel distribution with a delay exists. If one point at the 50 percentile had shifted, the median would have jumped from 12 to 16 seconds, past the 15 second specification.

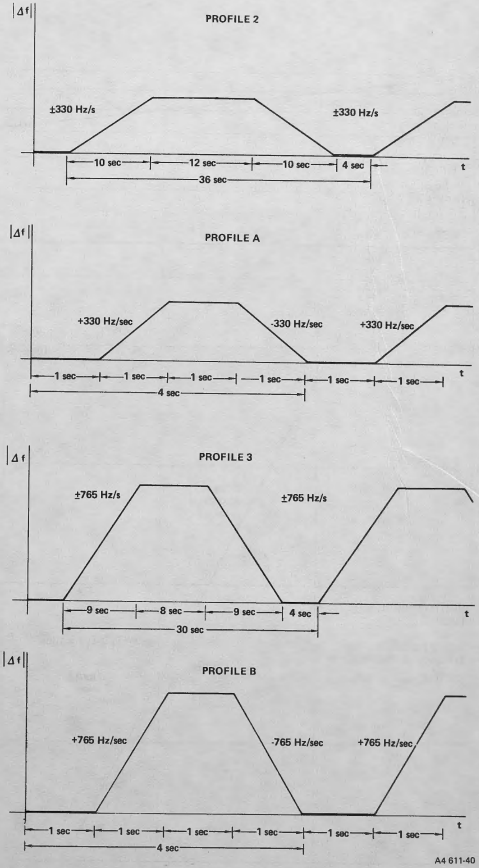

Figure 13. Loss-of-Lock Profiles. In all figures, the sharp corners stress a phase-lock-loop with an "infinite" jerk.

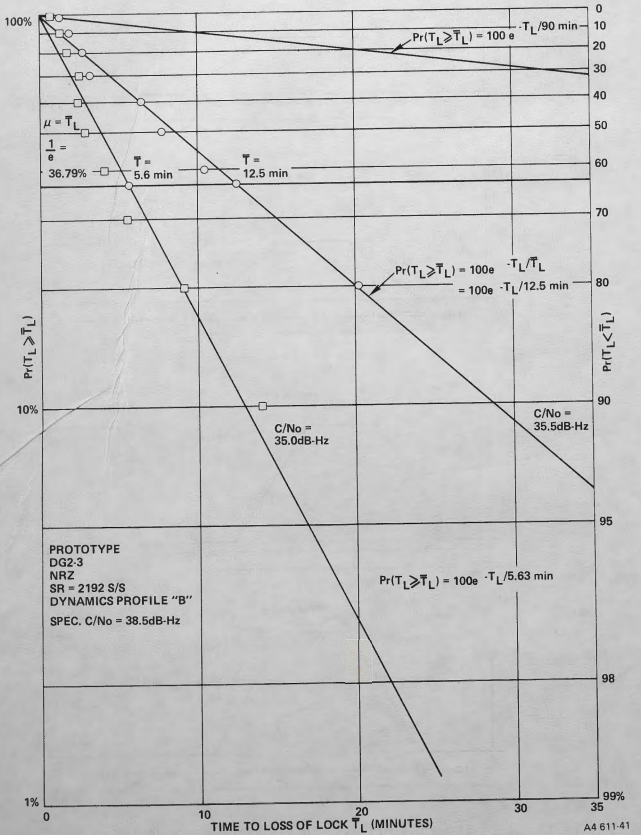

Figure 14. Exponential Distribution of Loss-of-Lock Times. The mean-time to loss-of-lock increases rapidly as the C/N_0 is increased.

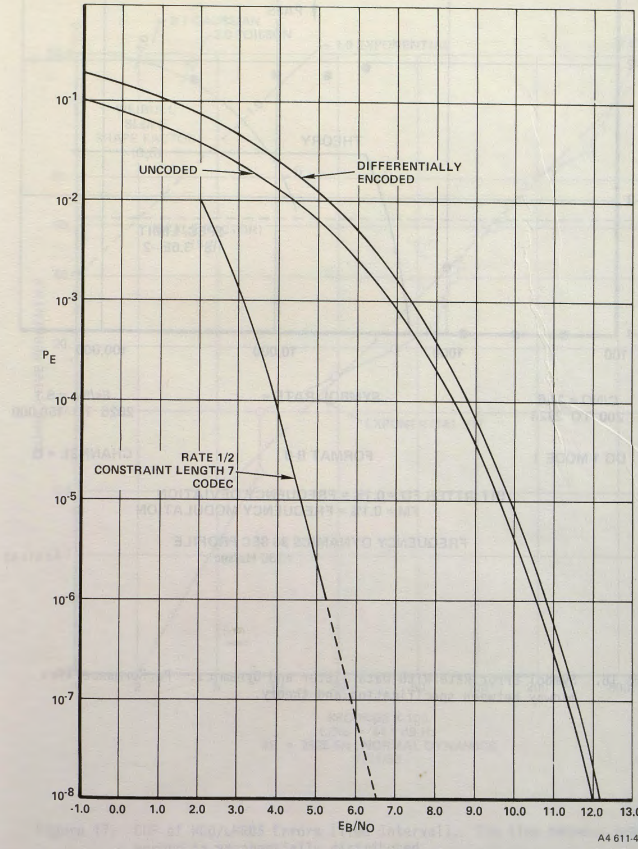

Figure 15. Theoretical BER Curve. WDD performance is about 1 dB worse than the theoretical "differentially encoded" curve.

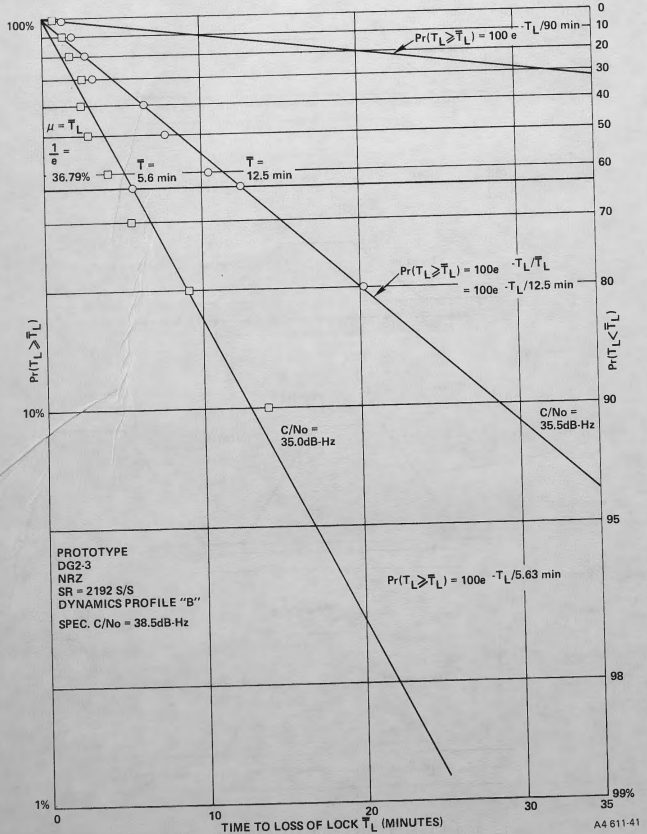

Figure 14. Exponential Distribution of Loss-of-Lock Times. The mean-time to loss-of-lock increases rapidly as the C/N_O is increased.

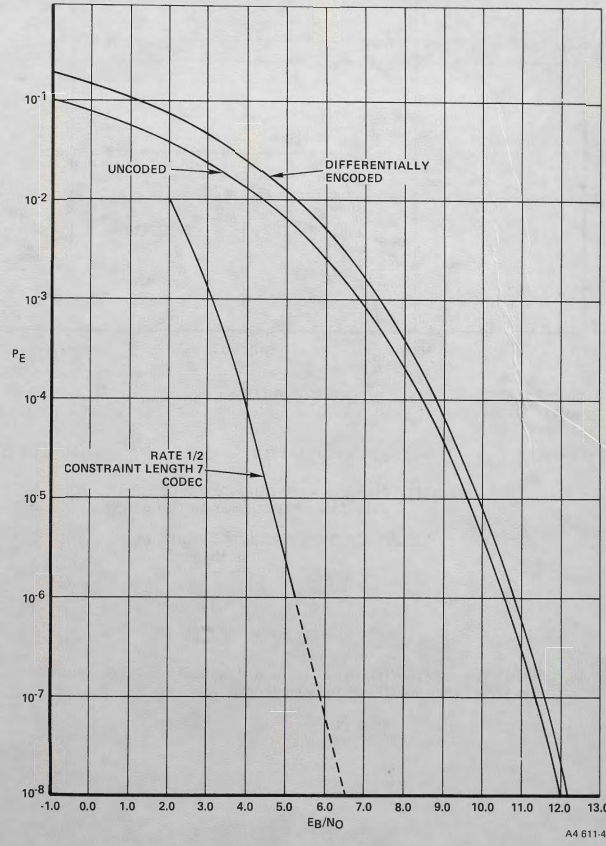

Figure 15. Theoretical BER Curve. WDD performance is about 1 dB worse than the theoretical "differentially encoded" curve.

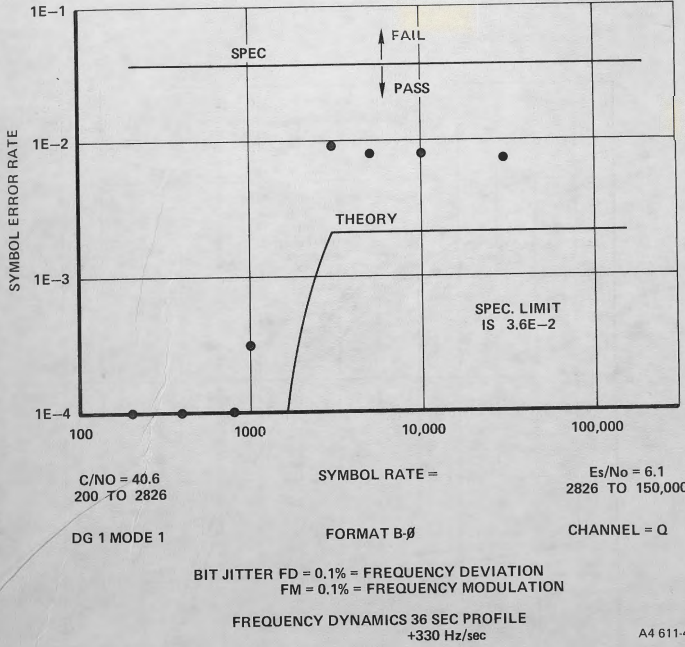

Figure 16. Symbol Error Rate With Data Jitter and Dynamics. Performance lies midway between specification and theory.

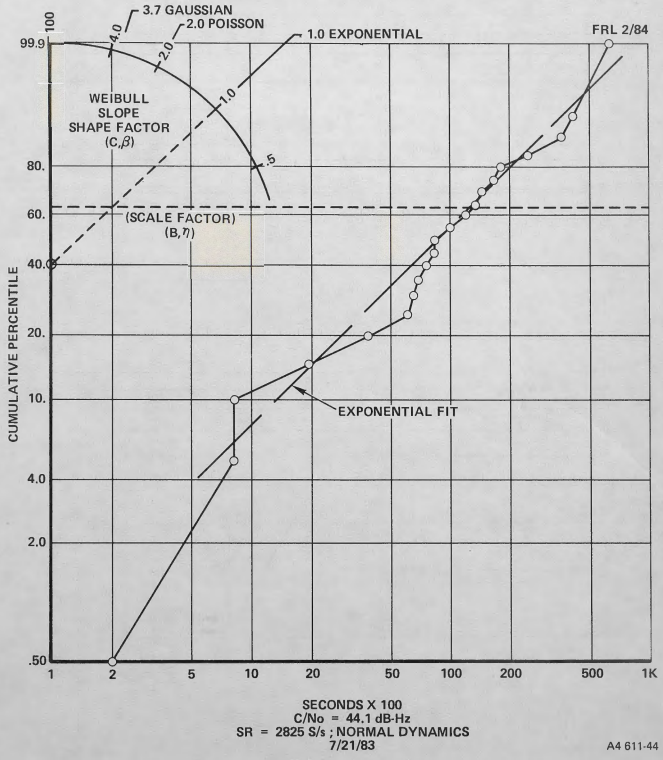

Figure 17. CDF of WDD/LMRBS Errors (Time Interval). The time between symbol errors is exponentially distributed.

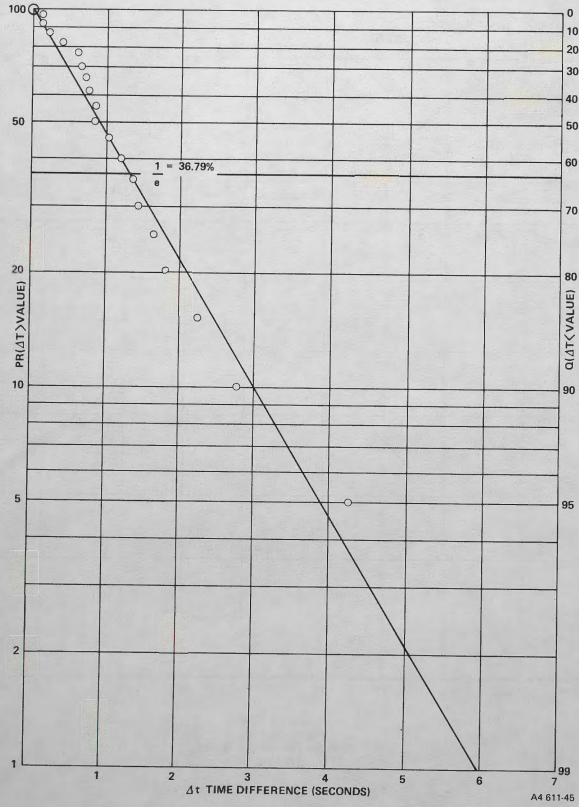

Figure 18. Δt Time Difference (Seconds). The time interval distribution is plotted on ordinary semi-log graph paper.

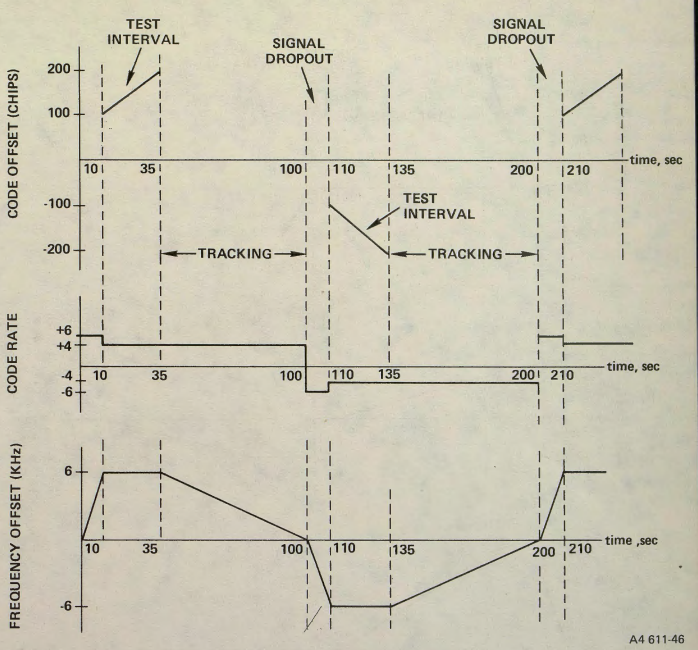

Figure 19. Test Profiles for Reacquisition With Maximum Rates. These STE dynamics force signal maximum rates of change.

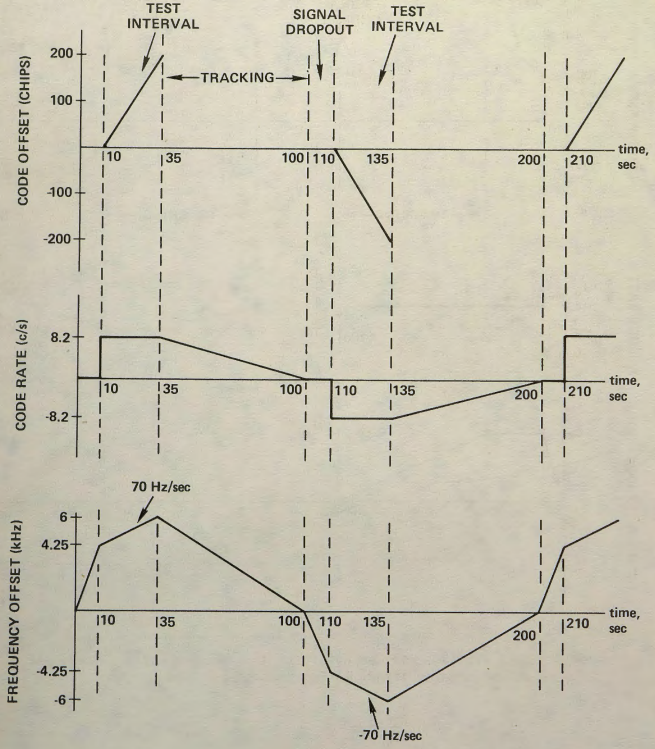

Figure 20. Test Profiles for Reacquisition With Maximum Offsets. These dynamics induce maximum offsets from the perfectly-corrected signal.

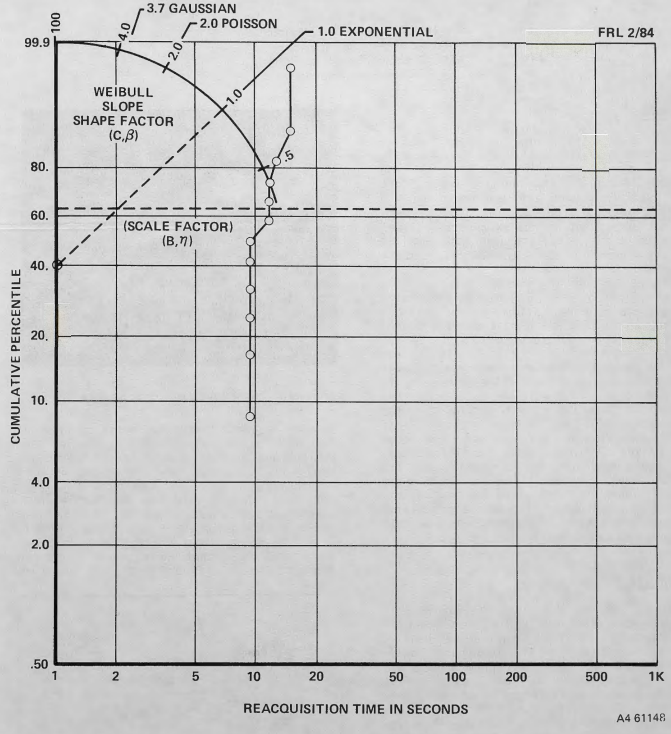

Figure 21. Reacquisition Time Cumulative Density Function (CDF). Reacquisition times show great consistency and are not exponentially distributed.